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Improved thermal stability of Sb materials by SiO₂ doping for ultra-fast phase change memory application



SiO2-doped Sb material is proved to be a promising candidate for phase change memory (PCM) use

because of its high crystallization temperature (~239 °C), large crystallization activation energy (4.05 eV),

and good data retention ability (162 °C for 10 years). The band gap is broadened and the grain size is

refined by SiO₂ doping. The reversible resistance transition can be achieved by an electric pulse as short

as 5 ns for the PCM cell based on SiO₂-doped Sb material. A lower operation power consumption (the

energy for RESET operation 1.1×10^{-11}]) is obtained. In addition, SiO₂-doped Sb material shows a good

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ABSTRACT

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1. Introduction

Phase change memory (PCM) has been considered one of the most promising contenders for the next generation nonvolatile memory owing to its excellent properties of excellent scalability, fast programming speed, cheap fabrication cost, logic compatibility and good cycle numbers [1,2]. The phase transition can be induced by the electrical pulse with nanosecond time scale, achieving pronounced resistance resolution to store the logic states "0" and "1" [3,4].

Among numerous phase change materials, Ge₂Sb₂Te₅ (GST) is the most widely utilized one because of its existing commercial applications in optical storage [5]. However, GST still has some areas for improvement, including the poor thermal stability as well as weak data retention [6,7]. Besides, the nucleation-dominated crystallization mechanism makes it difficult for the GST-based PCM devices to have an entire operating window when the width

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of the voltage pulse is shorter than 100 ns, which is insufficient to satisfy the requirement of dynamic random access memory (DRAM) (~10 ns) [8]. Therefore, many efforts are devoting to the development of new phase change materials to improve the performance of PCM. Thereinto, Sb-rich phase change materials have obtained much concern due to fast phase switching speed, such as Ga-Sb[9], C-Sb[10], Mg-Sb[11], Ti-Sb[12], Zn-Sb[13], Al-Sb[14], Si-Sb[15], Er-Sb[16] and SiC-Sb[17]. In this work, SiO₂ is selected as a dopant to improve the phase change property of Sb material because it has shown good effects in SiO₂-doped GST material [18]. The impacts of SiO₂-doping on thermal, optical and electrical properties were investigated in detail.

2. Experimental

Thin films of $(SiO_2)_xSb_{1-x}$ (x = 0.22, 0.28, 0.36, 0.40) were deposited on Si/SiO_2 substrate at room temperature via cosputtering SiO_2 and Sb pure targets. Sb films were also prepared by sputtering Sb pure target for comparison. The purities of all targets were 99.999% and the thickness was set to 50 nm by controlling the deposited time. The background pressure and work pressure of the sputtering system were 1.0×10^{-4} and 0.4 Pa,



endurance of 2.5 \times 10⁵ cycles.





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respectively. The compositions of the deposited films were determined by means of energy dispersive spectroscopy (EDS). The amorphous-to-crystalline transition was investigated by in situ film resistance measurements under an Ar atmosphere. The crystalline structures of (SiO₂)_xSb_{1-x} films with different SiO₂ content were analyzed by X-ray diffraction (XRD) carried out on a Bruker D8 Advanced diffractometer with Cu κ_{α} radiation in the 2 θ range from 20 to 60°, with a scanning step of 0.01°. The surface roughness of the films was evaluated by Atomic Force Microscope (AFM, FM-Nanoview 1000), which was carried out in the semi-contact mode. The PCM devices based on the SiO₂-doped Sb materials were fabricated and the electrical switching property was measured by a Tektronix AWG5012B arbitrary waveform generator and a Keithley 2400 m. A square-shape current pulse was injected into the cell and bypass line using a pulse generator. The current pulse was passed through a digital oscilloscope, which measured the pulse shape and amplitude that was applied to the cell with the series resistance of the oscilloscope.

3. Results and discussion

The change in resistance as a function of temperature for $(SiO_2)_xSb_{1-x}$ materials is shown in Fig. 1 with a heating/cooling rate fixed at 10 °C/min from room temperature to 280 °C and subsequent cooling. In the heating section, the resistance of all (SiO₂)_xSb_{1-x} materials decreases with increase of temperature, coupled with a rapid drop at crystalline temperature (T_c), which is due to the sharp increase of carrier density within the materials [19]. As the SiO₂ content goes up, the resistances of amorphous and crystalline states increase from 1.5 \times 10^{6} and 3 \times 10^{3} Ω of $(SiO_2)_{0.22}Sb_{0.78}$ to 6.9 \times 10^7 and 2.4 \times $10^4\Omega$ of $(SiO_2)_{0.40}Sb_{0.60}$ respectively. The higher resistance is helpful for reducing RESET current according to the joule heating equation: $Q = l^2 \cdot R \cdot t$, where *Q*, *I*, *R*, and *t* are the thermal energy, current, electrical resistance and time, respectively [20]. Besides, the T_c of $(SiO_2)_{0.22}Sb_{0.78}$ materials is about 195 °C. After more SiO₂ doping, the T_c increases to 209 °C of (SiO₂)_{0.28}Sb_{0.72}, 230 °C of (SiO₂)_{0.36}Sb_{0.64} and 237 °C of (SiO₂)_{0.40}Sb_{0.60}. By contrast, no obvious resistance change in heating process is observed for the pure Sb thin film, which indicates that some Sb crystalline phases could have formed in depositing process due to its poor amorphous thermal stability. Generally, the amorphous thermal stability can be roughly evaluated by the crystalline temperature. Therefore, the adding of SiO₂ inhibits the crystallization of Sb, resulting in better amorphous thermal stability.



Fig. 1. Resistance of $(SiO_2)_xSb_{1-x}$ films as a function of annealing temperature with the heating rate of 10 $^\circ C/min.$

$$K/S = (1-R)^2/(2R)$$
 (1)

Where *R* is the reflectivity, *K* is the absorption coefficient, and *S* is the scattering coefficient. The band gap energy of Sb, $(SiO_2)_{0.22}Sb_{0.78}$, $(SiO_2)_{0.28}Sb_{0.72}$, $(SiO_2)_{0.36}Sb_{0.64}$ and $(SiO_2)_{0.40}Sb_{0.60}$ thin films were 0.49, 0.59, 0.70, 0.80 and 0.88 eV, respectively. With the increase of SiO₂ concentration, the *E*_g of amorphous films is extended. Because the carrier density inside the semiconductors is proportional to $\exp\left(-\frac{E_g}{2kT}\right)$, an increase in the band gap will lead to the reduction of carriers, which makes a major contribution to the increasing of film resistivity after more SiO₂-doping [22]. This finding is supported by the change trends of resistance curves in Fig. 1.

In order to evaluate the data retention of phase change materials, the isothermal crystallization was employed in timedependent resistance at different temperatures. The change of normalized resistance with time for (SiO₂)_xSb_{1-x} thin films at isothermal annealing process was showed in Fig. 3 a-c. The failure time is defined as the time when the resistance reaches half of its initial value at a specific isothermal temperature. The typical inverse S-shaped growth curves can be seen for the isothermal crystallization, including incubation period, steady-state nucleation, growth, and coarsening [23]. For every sample, four isothermal temperatures are selected lower than the T_c . Fig. 3a shows that the failure time of (SiO₂)_{0.22}Sb_{0.78} thin film at the annealing temperature 193 °C is 286 s. Corresponding to lower annealing temperature 183 and 178 °C, the failure time increases to 844 and 1554 s, respectively. A lower isothermal temperature will result in a longer failure time because it needs more time to accumulate the energy for the nucleation and grain growth. The similar change trends could be obtained for (SiO₂)_{0.36}Sb_{0.64} and (SiO₂)_{0.40}Sb_{0.60} materials. What's more, the failure time for 215 °C annealed (SiO₂)_{0.40}Sb_{0.60} thin film is 3536 s, which is much longer than that of 213 °C annealed (SiO₂)_{0.36}Sb_{0.64} thin film (2385 s). Thus, the data retention is greatly improved by SiO₂ doping.

The plot of logarithm failure time vs. $1/(k_bT)$, which fits a linear Arrhenius relationship due to its thermal activation nature, can be described as [24]:



Fig. 2. The Kubelka-Munk function of Sb and (SiO₂)_xSb_{1-x} films.



Fig. 3. (a)-(c) The change of resistance with time for $(SiO_2)_xSb_{1-x}$ thin films at isothermal annealing process. (d) Arrhenius plots of failure time vs. 1/kT of $(SiO_2)_xSb_{1-x}$ thin films and the extrapolated data retention time at specified temperatures.

$$t = \tau_0 \exp[E_c / (k_b \times T)] \tag{2}$$

where t, τ_0 , E_c , k_b , and Tare failure time, the pre-exponential factor depending on the material's properties, the activation energy of crystallization, Boltzmann's constant and absolute temperature of concern, respectively. Fig. 3d shows that the 10-year lifetime for $(SiO_2)_{0.22}Sb_{0.78}$, $(SiO_2)_{0.28}Sb_{0.72}$, $(SiO_2)_{0.36}Sb_{0.64}$ and $(SiO_2)_{0.40}Sb_{0.60}$ materials are 113, 125, 154 and 162 °C, respectively, which are all higher than that of GST material (85 °C) [6]. Accordingly, the E_c for $(SiO_2)_{0.22}Sb_{0.78}$, $(SiO_2)_{0.28}Sb_{0.72}$, $(SiO_2)_{0.36}Sb_{0.64}$ and $(SiO_2)_{0.40}Sb_{0.60}$ materials are 2.65, 3.15, 3.66 and 4.05 eV, respectively. From this perspective, $(SiO_2)_xSb_{1-x}$ materials possess better reliability of the amorphous state to meet the application of data storage at elevated temperature.

Figs. 4 and 5 show the XRD patterns of pure Sb and $(SiO_2)_xSb_{1-x}$ materials annealed at different temperature for 10 min in Ar atmosphere. For pure Sb material in Fig. 4, a broad diffraction peak (110) of Sb phase belonging to rhomb-centered configuration can be seen in an as-deposited sample. It indicates that the crystallization has occurred in the as-deposited Sb material, which is in accord with the result of Fig. 1. With the increasing of annealing temperature, the crystal grains further grow with the intensity of peak (110) increasing. Being different from Sb, no obvious diffract peaks are observed for as-deposited and 120 °C annealed (SiO₂)_xSb_{1-x} materials, indicating the amorphous nature. In 204 °C



Fig. 4. XRD patterns of Sb thin films annealed at different temperatures for 10 min in Ar atmosphere.

annealed $(SiO_2)_{0.22}Sb_{0.78}$ material, two weak diffract peaks of Sb (110) and (015) appear, which demonstrates its better amorphous thermal stability than pure Sb material. For $(SiO_2)_{0.28}Sb_{0.72}$, $(SiO_2)_{0.36}Sb_{0.64}$ and $(SiO_2)_{0.40}Sb_{0.60}$ materials, the appearance of the new peak (012) further confirms the rhomb-centered Sb phase configuration. Besides, no SiO₂ diffraction peaks are observed in $(SiO_2)_xSb_{1-x}$ materials, indicating the doped SiO₂ exists in amorphous state. The intensity of diffraction peak (110) for $(SiO_2)_{0.40}Sb_{0.60}$ material is much weaker than that of pure Sb. It manifests that the crystallization of Sb in $(SiO_2)_xSb_{1-x}$ materials is restrained by amorphous SiO₂, which is conducive to improve the stability of Sb materials.

Phase change is accompanied by an induced stress which leads to a change of film surface roughness. Film surface roughness has a significant impact on device performance by affecting the quality of the electrode-film interface [25]. The AFM images of Sb and (SiO₂)_{0.40}Sb_{0.60} thin films before and after annealing are presented in Fig. 6. For as-deposited Sb thin film in Fig. 6a, the surface is smooth with the root-mean-square surface roughness of 0.672 nm. After annealed at 350 °C for 10 min, the roughness of Sb increases to 1.754 nm due to internal amorphous to crystalline phase transform. By contrast, the roughness change of (SiO₂)_{0.40}Sb_{0.60} thin film is relatively small. The (SiO₂)_{0.40}Sb_{0.60} thin film has a better flatness with the roughness change from 0.322 nm of amorphous state to 0.753 nm of crystalline state. This result also confirms the fact that SiO₂ doping inhibits the crystallization of the Sb thin film and improves the thermal stability, which is in accord with the XRD results in Figs. 4 and 5.

T-shaped PCM device was fabricated to verify the electrical switching behavior of (SiO₂)_{0.40}Sb_{0.60} thin film. Schematic diagram of a PCM cell is shown in Fig. 7a inset, in which the semimanufactured cell with 190 nm W plug for depositing (SiO₂)_{0.40}Sb_{0.6} ofilm (50 nm), TiN (10 nm), and Al (300 nm) layers was prepared through 130 nm complementary metal oxide semiconductor (CMOS) technology. The R-V characteristics demonstrate that completely reversible SET/RESET operations can be realized by voltage pulses of different widths. A voltage pulse with a narrower width will need a higher threshold voltage to excite the resistance switching. In the reversible operations, the SET operation needs less power but a much longer time than the RESET operation. Hence, we pay more attention to the set speed and reset power. Fig. 7a shows that the (SiO₂)_{0.40}Sb_{0.60}-based PCM device can switch completely with a pulse of only 5 ns. In contrast, the PCM cells based on GST films are difficult to switch in the pulse of 100 ns, which verifies the fast transformation speed of (SiO₂)_{0.40}Sb_{0.60} thin film. It is reported



Fig. 5. XRD patterns of (a) (SiO₂)_{0.22}Sb_{0.78}, (b) (SiO₂)_{0.28}Sb_{0.72}, (c) (SiO₂)_{0.36}Sb_{0.64}, (d) (SiO₂)_{0.46}Sb_{0.60} thin films annealed at different temperatures for 10 min in Ar atmosphere.



Fig. 6. AFM measurements of as-deposited and annealed Sb and $(SiO_2)_{0.40}Sb_{0.60}$ thin films.

that Sb-rich phase-change materials have a growth-dominated crystallization behavior rather than a nucleation-dominated one

[20]. In the crystallization process, the dispersed Sb-Sb bonds are easily broken and can act as heterogeneous nucleating agents to



Fig. 7. (a) *R-V* performance of the PCM cell based on $(SiO_2)_{0.40}Sb_{0.60}$ and GST thin films. Inset shows the cross-sectional cell structure of PCM device. (b) The endurance characteristic of $(SiO_2)_{0.40}Sb_{0.60}$ -based cell devices.

improve the switching speed. The RESET voltage of $(SiO_2)_{0.40}Sb_{0.60}$ (2.2 V for 5 ns pulse) is much smaller than that of GST (3.6 V for 500 ns pulse). The necessary energy for RESET operation E_{reset} is estimated by $V_{reset}^2/R_{reset} \times t_{reset}$ Ref. [26]. The power consumption for the RESET operation of $(SiO_2)_{0.40}Sb_{0.60}$ cell is calculated to be around 1.1×10^{-11} J, which is ten times lower than that of GST cell (9.6 $\times 10^{-10}$ J). The pulse width of 300 ns rated at 0.6 and 1.5 V was alternately applied for set and reset operations, respectively. As is shown in Fig. 7b, the reversible switching up to 2.5×10^5 cycles without failure is achieved. The good endurance character further demonstrates the practicability of SiO₂-doped Sb thin films in the PCM devices.

4. Conclusions

In summary, SiO₂-doped Sb material was investigated for use as an appropriate phase-change material in PCM. SiO₂-doped Sb materials have better amorphous thermal stability ($(SiO_2)_{0.22}Sb_{0.78}$: T_c 195 °C, E_c 2.65 eV; $(SiO_2)_{0.28}Sb_{0.72}$ T_c 209 °C, E_c 3.15 eV; $(SiO_2)_{0.36}Sb_{0.64}$ T_c 230 °C, E_c 3.66 eV; $(SiO_2)_{0.40}Sb_{0.60}$: T_c 237 °C, E_c 4.05 eV). The $T_{10-year}$ of $(SiO_2)_{0.36}Sb_{0.64}$ and $(SiO_2)_{0.40}Sb_{0.60}$ materials reached to 154 and 162 °C, respectively. The band-gap widths of the amorphous Sb film were extended after more SiO₂ doping. The surface roughness of crystalline Sb and $(SiO_2)_{0.40}Sb_{0.60}$ films were 1.754 and 0.753 nm, respectively. The reversible resistance transition was achieved by an electric pulse as short as 5 ns for $(SiO_2)_{0.40}Sb_{0.60}$. Compared with GST, the $(SiO_2)_{0.40}Sb_{0.60}$ -based PCM device had a lower E_{reset} of 1.1 × 10⁻¹¹ J. The reversible switching of 2.5 × 10⁵ cycles was achieved. These results demonstrate that the SiO₂-doped Sb material is a promising candidate for high stability and high-speed PCM applications.

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